

Description

[GATE STRUCTURE FORMING METHOD OF FIELD EFFECT TRANSISTOR]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a fabrication method for a semiconductor device. More particularly, the present invention relates to a fabrication method for a gate structure of field effect transistor (FET).

[0003] Description of Related Art

[0004] The metal semiconductor field effect transistor (MESFET) or the high electron mobility transistor (HEMT) is a microwave device. In order to increase the operation frequency and efficiency, reducing the gate length and suppressing the signal noise are feasible approaches. However, as devices enter the sub-micron stage, the resistance of the gate increases as the gate length reduces. In order to overcome the aforementioned problem, a T-

shaped gate structure technique is widely used. Further, simpler manufacturing techniques are also being developed.

[0005] Figures 1A to 1D are schematic, cross-sectional diagrams illustrating a process flow for fabricating a T-shaped gate structure according to the prior art.

[0006] Referring to Figure 1A, a photoresist layer 102 and a photoresist layer 104 are formed on a substrate 100. An electron beam exposure process 106 is then conducted on the photoresist layer 102 and the photoresist layer 104, wherein the energy of the main beam 106a is greater than the energy of the side beam 106b.

[0007] Referring to Figure 1B, a two-step development process is conducted to form the patterned photoresist layer 102a and the patterned photoresist layer 104a, wherein at the region where the electron beam 106a (higher energy) is directed to, both photoresist layers 102a, 104a are being developed, whereas at the region where the electron beam 106b (lower energy) is directed to, only the photoresist layer 104a is being developed.

[0008] Referring to Figure 1C, a metal evaporation deposition process is conducted to form a metal layer 108 on the exposed surface of the substrate 100 and on the photoresist

layers 102a, 104a, wherein the metal layer 108a that is formed on the substrate 100 surface and the photoresist layer 102a is separated from the metal layer that is formed on the photoresist layer 104a.

[0009] Continuing to Figure 1D, the photoresist layers 102a, 104a are removed. Concurrently, the metal layer 108b is also being striped, leaving only the metal layer 108a to form a T-shaped gate structure.

[0010] However, in the aforementioned method, the fabrication of the gate structure requires the application of the electron beam development process. The manufacturing cost is thus higher and a lower throughput is resulted (1 to 2 wafer per hour). Further, seam may be generated on the surface of the subsequently formed metal layer (gate structure) when the rounding of the lower photoresist layer profile is not sufficient. The reliability of the device is thus affected.

[0011] Figures 2A to 2D are schematic, cross-sectional diagrams illustrating a process flow for fabricating another type of gate structure.

[0012] As shown in Figure 2A, a patterned silicon nitride layer 202 is formed on a substrate 200, exposing a part of the substrate 200. A photoresist layer 204 is then formed

over the silicon nitride layer 204.

[0013] Referring to Figure 2B, a photolithography process is conducted to pattern the photoresist layer 204 to form the photoresist layer 204a. The photoresist layer 204a exposes a part of the silicon nitride layer 202 and a substrate 200 surface exposed by the silicon nitride layer 202.

[0014] Continuing to Figure 2C, a metal evaporation deposition process is conducted to form a metal layer 206 on the photoresist layer 204a, the exposed silicon nitride layer 202 and the substrate 200 surface, wherein the metal layer 206b formed on the photoresist layer 204a is separated from the metal layer 206a on the silicon nitride layer and the substrate 200 surface.

[0015] Referring to Figure 2D, the photoresist layer 204a is removed. Concurrently, the metal layer 206b is striped, leaving only the metal layer 206a to serve as a T-shaped gate structure.

[0016] However, when a gate structure is formed with the above methods, parasitic capacitance is formed between the gate, the silicon nitride layer and the substrate due to a direct contact between the top surface of the silicon nitride layer and the substrate. The presence of a parasitic

capacitance lowers the cutoff frequency and the maximum transition frequency. As a result, noise interference increases during the operation of the device.

SUMMARY OF INVENTION

[0017] Accordingly, the present invention provides a fabrication method for a gate structure, wherein the deficiencies in the conventional manufacturing method for a T-shaped gate structure, for example, high cost and low yield, are resolved.

[0018] The present invention also provides a fabrication method for a gate structure, wherein the generation of parasitic capacitance at the gate formed according the conventional manufacturing method for a T-shaped gate structure is resolved.

[0019] The present invention further provides a fabrication method for a metal semiconductor field effect transistor, wherein the reliability of a device is improved and a better operation efficiency is resulted.

[0020] The present invention provides a fabrication method for a gate structure, wherein a pad layer is formed on a surface of a substrate. A patterned first photoresist layer is formed on the pad layer, wherein the patterned first photoresist layer exposes the pad layer. An ultra-violet curing

step is conducted to form a cross-linked layer at the surface of the first photoresist layer. Thereafter, a rounding step is conducted for rounding the profile of the first photoresist layer. The pad layer that is not covered by the first photoresist layer is then removed to expose a surface of the substrate. A patterned second photoresist layer is then formed on the first photoresist layer, wherein the second photoresist layer exposes a part of the first photoresist layer and the substrate surface that is being exposed by the first photoresist layer. A deposition step is conducted to form a conductive layer on the second photoresist layer, the first photoresist layer and the surface of the substrate, wherein the conductive layer formed on the second photoresist layer is separated from the metal layer formed on the first photoresist layer and the substrate surface. The first photoresist layer and the second photoresist layer are then removed, wherein the conductive layer formed on the second photoresist layer is concurrently striped, and the remaining conductive layer serves as a gate.

[0021] Thereafter, the pad layer is then patterned. Subsequent to the formation of a source/drain region on the surface of the substrate, a metal semiconductor field effect transis-

tor is formed.

[0022] Since the T-shaped gate structure formed according to the present invention is not in a direct contact with the top surface of the pad layer, the generation of parasitic capacitance as in the conventional technique is thus prevented.

[0023] Further, in the fabrication method for a gate structure of the present invention, expensive and low yield manufacturing apparatus are precluded. The present invention thus provides a low cost and high yield manufacturing method for a gate structure.

[0024] Further, the gate electrode of the metal semiconductor field effect transistor of the present invention is a T-shaped gate electrode, which has a low resistance and no parasitic capacitance. The reliability and the operation efficiency of the device of the present invention are thereby desirable.

[0025] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0026] The accompanying drawings are included to provide a

further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0027] Figures 1A to 1D are schematic, cross-sectional diagrams illustrating a process flow for fabricating for a T-shaped gate structure according to the prior part.

[0028] Figures 2A to 2D are schematic, cross-sectional diagrams illustrating a process flow for fabricating for a T-shaped gate structure according to another prior part.

[0029] Figures 3A to 3H are schematic cross-sectional diagrams illustrating a process flow for fabricating a field effect transistor according to one aspect of the present invention.

DETAILED DESCRIPTION

[0030] Figures 3A to 3H are schematic cross-sectional views showing a fabrication process flow for a field effect transistor according to one aspect of the present invention.

[0031] Referring to Figure 3A, a pad layer 302 is formed on a substrate 300, wherein the substrate is, for example, a gallium arsenate (GaAs) substrate, and the pad layer 302 is used to prevent the surface of the substrate from being

damaged in the subsequent process. The pad layer 302 is about, for example, 500 angstrom to 2000 angstroms thick, preferably between 500 angstroms to 1000 angstroms thick. The pad layer 302 is formed with, for example, silicon nitride, silicon oxide, silicon oxynitride or other combination. Thereafter, an anti-reflection layer 304 and a photoresist layer 306 are sequentially formed on the pad layer 302, wherein the photoresist layer 306 comprises an opening 308, and the dimension of the opening 308 is determined according to the dimension of the subsequently formed gate structure.

[0032] Forming the anti-reflection layer 304 and the photoresist layer 306 includes, spin-coating a layer of an anti-reflection material (not shown) on the substrate 300 at a speed of 5500 rpm, and baking at a temperature 190 degrees Celsius for about 60 seconds to form the anti-reflection layer 304. Thereafter, a layer of photoresist material (not shown) is spin-coated on the anti-reflection layer 304 at a speed of 6000 rpm, followed by baking at a temperature of 100 degrees for 60 seconds. An exposure and development process is further conducted to form the photoresist layer 306 with an opening 308. The wavelength of the exposure light source used in the exposure

process is, for example, 436nm, 365nm, 248nm or 193 nm. The anti-reflection layer 304 is used to absorb the light that is not being absorbed by the photoresist material layer during the exposure process to prevent the generation of a standing wave. The anti-reflection layer 304 is about 700 angstroms to 900 angstroms thick. The anti-reflection layer 304 is, for example, an organic anti-reflection layer or an inorganic anti-reflection layer (for example, silicon nitride or silicon oxynitride). In this aspect of the invention, an organic anti-reflection layer is used for the illustration. The photoresist layer 306 is about, for example, 3000 angstroms to about 10000 angstroms thick. Further, the photoresist layer 306 can be a positive photoresist or a negative photoresist.

[0033] Referring to Figure 3B, a cross-linked surface layer 309 is formed at the surface of the photoresist layer 306. The cross-linked surface layer 309 is a hard layer and is insensitive to the subsequent lithographic process. Forming the cross-linked surface layer 309 includes, for example, performing an UV curing treatment on the photoresist layer 306. Further, during the process of the UV curing treatment to form the cross-linked surface layer 309, the underlying photoresist layer 306 is prevented from being

scratched and thus remains complete. In a preferred exemplary embodiment, the UV-curing treatment is conducted with energy of about, for example $200\text{mw}/\text{cm}^3$, at a temperature of about 100 degrees to 130 degrees Celsius. Further, the UV curing treatment is conducted for, for example, about 30 seconds to 60 seconds, wherein the duration of the treatment depends on the energy and the temperature of the UV curing treatment.

[0034] Referring to Figure 3C, a rounding process is conducted to transform the original right angle profile of the photoresist layer 306a to a rounding profile. If the profile of the photoresist layer 306a is sufficiently rounded, the prevention of the generation of seam in the subsequently formed gate structure is enhanced. The above rounding step is achieved by, for example, conducting an ion-milling or a thermal flowing baking process, wherein the desirable rounding profile for the photoresist layer can be achieved by adjusting the injection angle of ions in the ion-milling process or by using a hot plate or an oven in the thermal flowing baking process.

[0035] Subsequent to the profile rounding of the photoresist layer 306a, the anti-reflection layer 304 and the pad layer 302 are etched to form a patterned anti-reflection layer

304a and a patterned pad layer 302a, and to form an opening 308a that exposes the substrate 300 surface, using the photoresist layer 306a as an etching mask. In one preferred exemplary embodiment, the anti-reflection layer 304 and the pad layer 302 are etched by, for example, using an ion coupled plasma etching apparatus and an oxygen gas as a reaction gas to etch the anti-reflection layer 304, followed by etching the pad layer 302.

[0036] One point that is worth mentioning is that the dimension d1 of the opening 308a that exposes the substrate 300 surface is the critical dimension of the subsequently gate structure. Therefore, during the etching process of the pad layer 302, the dimension d1 can be adjusted to achieve the expected target dimension.

[0037] Referring to Figure 3D, a photoresist layer 310 is formed above the substrate 300, covering the photoresist layer 306a and filling the opening 308a. The photoresist layer 310 can be a positive photoresist or a negative photoresist. The photoresist layer 310 is formed by, for example, spin-coating a layer of photoresist material (not shown) at a speed of 2000rpm, followed by baking at 90 degrees Celsius for about 60 seconds to form the photoresist layer 310 of about 10000 angstroms to about 25000

angstroms thick.

[0038] Continuing to Figure 3E, an exposure and development process is conducted to pattern the photoresist layer 310 to form a photoresist layer 310a with an opening 311, wherein the opening 311 corresponds to where the opening 308a is previously formed. Further, the dimension (width) d2 of the opening 311 is greater than the dimension (width) d1 of the opening 308a that exposes the substrate 300 surface. Preferably, the dimension d2 of the opening 311 is least twice as big as the dimension d1 of the opening 308a that exposes the substrate 300 surface. As a result, a portion of the photoresist layer 306a and the substrate 300 surface are exposed by the opening 311.

[0039] More particularly, the photoresist layer 310a is formed having an opening 311, wherein the sidewall of the opening 311 and the sidewall of the opening 308a forms an acute angle. To form the opening 311 of the photoresist layer 310, wherein the sidewall of the opening 311 and the sidewall of the opening 308a forms an acute angle includes using a negative photoresist as a material for the photoresist layer 310 to perform the exposure and development process or using an image reverse (IR) photoresist

as a material for the photoresist layer 310 to perform the exposure and development process, or using a positive photoresist as a material for the photoresist layer 310 to perform the exposure and development process after a special treatment step.

[0040] Referring to Figure 3F, a metal layer 312 is formed on the photoresist layer 310a, the photoresist layer 306a and the substrate 300 surface, wherein the metal layer 312 can be any known, appropriate metal material. The metal layer 312 is formed by, preferably, a directional deposition method, for example, an evaporation deposition method, a sputtering method, an electroplating method. Since the sidewall of the opening 311 and the sidewall of the opening 308a forms an acute angle, the metal layer 312b formed on the surface of the photoresist layer 310a by an evaporation method is not connected to the metal layer 312a formed on the photoresist layer 306a and the substrate 300 surface. In fact, the metal layer 312b is separated from the metal layer 312a.

[0041] In a preferred exemplary embodiment, the evaporation deposition method includes performing a descum step, which is a descum using an oxygen plasma for about two minutes under a power source of 1000 watts and a pres-

sure of 0.5 torr, followed by wetting with an acid and water (1:20) mixture solution for 20 seconds, and then drying for 30 seconds with air. A metal evaporation deposition step is then conducted to form a metal layer 312, wherein the metal layer 312 includes titanium of 250 angstroms thick, platinum of 250 angstroms thick and gold of 5000 angstroms thick.

[0042] Referring to Figure 3G, the photoresist layer 310a, the photoresist layer 306a and the anti-reflection layer 304a are removed. Further, the metal layer 312b is concurrently striped to expose the pad layer 302a. Removing the photoresist layers 310a, 306a and the anti-reflection layer 304a includes, for example, using a wet etching method. Since the metal layer 312b formed on the surface of the photoresist layer 310a is separated from the metal layer 312a, the metal layer 312b is also being striped during the removal of the photoresist layers 310a, 306a and the anti-reflection layer 304a, leaving only the metal layer 312a to form the gate structure of the present invention. Further, the gate structure of the present invention will not be in direct contact with the top surface of the pad layer 302a.

[0043] Continuing to Figure 3H, the pad layer 302a is patterned

to form the pad layer 302b, and a source region / drain region 314a/314b is then formed on the substrate 300 to complete a fabrication of a transistor. The source/drain region 314a/314b is formed with, for example, a metal material.

[0044] Using the aforementioned method for fabricating a transistor, when the gate length is about 0.35 micron, the average value for the cutoff frequency, detected by $V_p-1.0$ volt, is about 38 ± 2 GHz.

[0045] In accordance to the fabrication method for the present invention, since the T-shaped gate structure of the present invention is not in a direct contact with the top surface of the pad layer, the generation of parasitic capacitance as in the prior art is prevented.

[0046] Further, in the fabrication method for a gate structure of the present invention, expensive and low yield manufacturing apparatus are precluded. The present invention thus provides a low cost and a high yield fabrication method.

[0047] Since, the gate of the field effect transistor of the present invention is a T-shaped gate structure that has a low resistance, the generation of parasitic capacitance is obviated to ensure the reliability and the efficiency of the de-

vice.

[0048] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.